REMARKS

This is a full and timely response to the non-final Official Action dated **March 15, 2011** (the "Office Action" or "Action"). Reconsideration of the application in light of the above amendments and the following remarks is respectfully requested.

Claim Status

By the preceding amendment, claims 11-12, 14, and 16-18 have been amended, and claim 10 has been cancelled without prejudice or disclaimer. Consequently, claims 1-9 and 11-20 are pending for further action.

Allowable Subject Matter

In the recent Office Action, the Examiner indicated the presence of allowable subject matter in claim 2. (Action, pp. 19-20). Applicant wishes to thank the Examiner for this finding of allowable subject matter.

Applicant agrees with the Examiner's conclusions regarding patentability, without necessarily agreeing with or acquiescing in the Examiner's reasoning. In particular, Applicant believes that the indicated claims, and the application in general, are allowable because the prior art fails to teach, anticipate or render obvious the invention as claimed, independent of how the claims or claimed subject matter may be paraphrased.

Objection to the Drawings

The drawings stand objected to under 37 C.F.R. § 1.83(a) as allegedly failing to show every technical feature specified in the claims. Specifically, the Examiner believes that the drawings do not show all of the subject matter of dependent claim 10. While Applicant still disagrees with the Examiner's reasoning in this regard, claim 10 has been cancelled in the spirit of cooperation and to expedite prosecution of the application. Consequently, the objection to the drawings is rendered moot and should be withdrawn.

Prior Art

1. Claim 11 stands rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by U.S. Patent No. 6,202,110 to Coteus et al. ("Coteus"). For at least the following reasons, this rejection is improper and should be reconsidered and withdrawn.

Claim 11 recites:

> An Application-Specific Integrated Circuit (ASIC), comprising:
> ***interface circuitry configured to communicate with a plurality of application-specific controller subsystems external to said ASIC***;
> interface circuitry configured to communicate with a plurality of general-purpose processors external to said ASIC; and
> ***controller circuitry communicatively configured to couple each said application-specific controller subsystem to at least one corresponding said general-purpose processor such that said at least one corresponding general-purpose processor performs processing on behalf of that said application-specific controller subsystem***.

(Emphasis added).

Support for the amendment to claim 11 can be found in Applicant's specification at, for example, page 4 lines 5-25.

Applicant notes that "[t]he examiner bears the initial burden . . . of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). In a rejection made under § 102, this burden is substantial, as a *prima facie* case of anticipation requires a demonstration that "*each and every element* as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987) (emphasis added); *see* M.P.E.P. § 2131.

The Federal Circuit has further clarified that "unless a reference discloses within the four corners of the document *not only all of the limitations claimed but also all of the limitations arranged or combined in the same way as recited in the claim*, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. § 102." *Net MoneyIN, Inc. v. Verisign, Inc.*, 545 F.3d 1359, 1371, 88 U.S.P.Q.2d 1751, 1759 (Fed. Cir. 2008) (emphasis added).

In light of these considerations, the recent Office Action does not meet the requisite burden to establish that the cited prior art anticipates claim 11. Specifically, Coteus fails to teach or suggest "interface circuitry configured to communicate with a plurality of application-specific controller subsystems external to said ASIC" or "controller circuitry communicatively configured to couple each said application-specific controller subsystem to at least one corresponding said general-purpose processor such that said at least one corresponding general-purpose processor performs processing on behalf of that said application-specific controller subsystem." (Claim 11).

Coteus is directed to a "computer construction" in which memory cards are mounted back-to-back on a backplane board. (Coteus, col. 1 lines 6-8, col. 1 lines 56-64). Incident to this construction, Coteus discloses a system in which a memory controller made up of two separate integrated circuits connects an I/O bus to a CPU bus. (Coteus, Fig. 3 and related text). The Action cites to this portion of Coteus as evidence that Coteus reads on the subject matter of claim 11. Applicant respectfully disagrees.

Claim 11 recites "interface circuitry configured to communicate with a plurality of application-specific controller subsystems external to said ASIC." The integrated circuits of Coteus are coupled to an I/O bus, which communicates with multiple I/O devices, but Coteus does not teach or suggest that the I/O devices are "application-specific *controller* subsystems." (Claim 11) (emphasis added).

Furthermore, the control integrated circuit taught by Coteus fails to teach or suggest controller circuitry that couples each application-specific controller subsystem to at least one corresponding general-purpose processor "such that said at least one corresponding general-purpose processor performs processing on behalf of that said application-specific controller subsystem." (Claim 11). While the control integrated circuit of Coteus is connected to a CPU bus of CPUs, Coteus never teaches or suggests that any of the processors connected to the CPU bus perform processing on behalf of any other device in communication with the control integrated circuit. (*See* Coteus, Figs. 1, 3, and related text). While certain I/O devices may provide data to and receive data from the CPUs of Coteus, this does not mean that the CPUs are performing processing for the I/O devices. (*See* claim 11). Indeed, this subject matter is completely outside the scope of Coteus.

Again, "[a] claim is anticipated [under 35 U.S.C. § 102] only if *each and every element* as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros.*, 814 F.2d at 631, 2 U.S.P.Q.2d at 1053 (emphasis added); *see NetMoneyIN*, 545 F.3d at 1371, 88 U.S.P.Q.2d at 1759; M.P.E.P. § 2131. Thus, Coteus cannot anticipate claim 11 because, for the above reasons, each and every element recited in claim 11 is not expressly or inherently found in Coteus. Consequently, the rejection of claim 11 and its dependent claims based on Coteus should be reconsidered and withdrawn.

2. Claims 1 and 7-8 stand rejected under 35 U.S.C. § 103(a) as being allegedly obvious over the alleged admitted prior art in view of U.S. Patent Application Publication No. 2004/0225778 by Borkar et al. ("Borkar"). For at least the following reasons, this rejection is improper and respectfully traversed.

Claim 1

Claim 1 recites:

> A circuit in an embedded processing system covering a number of technical applications, a number of operative functions of the number of technical applications being performed via a respective number of application-specific Electronic Control Units (ECU), the circuit comprising:
>
> a) a number of controller means for controlling respective application specific ECUs, each of the controller means comprising a number of application-specific support functions and I/O subsystems; and
>
> b) a number of processor units each having an I/O-interface operatively connecting to a respective one of the controller means ***and supplying that controller means with computing power***,
>
> ***wherein at least one of the processor units and a respective controller means are implemented on different chips***.

(Emphasis added).

Applicant again respectfully notes that "[t]he examiner bears the initial burden . . . of presenting a *prima facie* case of unpatentability." *Oetiker*, 977 F.2d at 1445, 24 USPQ2d at1444. A *prima facie* case of obviousness made under 35 U.S.C. § 103(a) requires a showing that all of the subject matter in the claim at issue would be obvious to one having ordinary skill in the art based on the teachings of the cited prior art at the time of invention. *See* M.P.E.P. § 2143.

The recent Office Action does not make a *prima facie* case of obviousness against claim 1 because it fails to provide sufficient evidence that the alleged admitted prior art in view of Borkar would render obvious the subject matter of claim 1 to one having ordinary skill in the art at the time of the invention. Specifically, the alleged admitted prior art and Borkar do not teach or suggest that "at least one of the processor units and a respective controller means are implemented on different chips," where each of a plurality of processing units "ha[s] an I/O-interface operatively connecting to a respective one of the controller means and suppl[ies] that controller means with computing power." (Claim 1).

The alleged admitted prior art is the "Description and Disadvantages of Prior Art" section of Applicant's specification. This section teaches that prior art electronic control units include "quite specialised expensive components" where "a dedicated single- or multiprocessor unit" is applied "to achieve one particular function" for a specific electronic control unit. (Specification, "Description and Advantages of Prior Art."). The alleged admitted prior art does not teach or suggest anywhere that "at least one of the processor units and a respective controller means are implemented on different chips." (Claim 1).

In this regard, the Action cites to Borkar, which discloses "a memory system in which controller IC0 is a memory controller (either part of a processor chip or in a different chip from

the processor)." (Borkar, para. 0004) (parentheses original). The Action cites to this portion of Borkar as evidence that Borkar teaches that "at least one of the processor units and a respective controller means are implemented on different chips." (Action, pp. 5-6). However, this conclusion is inaccurate. Borkar refers simply to a processor that interacts with a memory controller to read from and write to memory controlled by the memory controller.

By contrast, claim 1 recites a "number of processor units each having an I/O interface operatively connecting to a respective one of the controller means ***and supplying that controller means with computing power***." (emphasis added). Because the processor of Borkar does not supply the memory controller with computing power, the processor and memory controller of Borkar are not analogous to the "number of processor units" and "controller means" recited in claim 1. Because Borkar is not from the same field of endeavor of the system in claim 1, and is not reasonably pertinent to the particular problem with which claim 1 is concerned, Borkar cannot reasonably be considered analogous art to claim 1. *See* 35 U.S.C. § 103; *In re Clay*, 966 F.2d 656 (1992) (analogous art under 35 U.S.C. § 103 must be either from the same field of endeavor or reasonably pertinent to the particular problem with which the inventor is involved). Thus, Borkar does not teach or suggest that "at least one of the processor units and a respective controller means are implemented on different chips," as those terms are used in claim 1.

The Action further asserts that it would have been obvious to one having ordinary skill in the art to implement respective controller means and processor units on different chips "because it would merely be an alternative arrangement or choice of design that would not affect the functionality of the invention." (Action, p. 5). Applicant strongly disagrees.

The Board of Patent Appeals and Interferences has refused to uphold rejections in which the examiner simply alleged that the relevant feature of a claimed invention is a mere "design choice." Such a statement, in the words of the Board, "is a conclusion, rather than a reason." *Ex parte Garrett*, 1986 Pat. App. LEXIS 8, 4 (BPAI 1986). Furthermore, the Federal Circuit has noted that "[t]o imbue one of ordinary skill in the art with knowledge of the invention [at issue], when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effects of a hindsight syndrome." *In re Fine*, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (quoting W.L. Gore & Assoc. v. Garlock, Inc., 220 USPQ 303, 312-13 (Fed. Cir. 1983)).

In a recent case at appeal, the Board of Appeals and Interferences reversed a rejection made based on an assertion of "mere design choice," noting that such an assertion amounts to a *per se* rule of unpatentability, which is "legally incorrect" and "inconsistent with section 103, which, according to *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966) and its progeny, entitles an applicant to issuance of an otherwise proper patent unless the PTO establishes that the invention as claimed in the application is obvious over cited prior art, based on the specific comparison of that prior art with claim limitations." *Ex parte Pennell*, Appeal 2009-009274, (B.P.A.I. Dec. 7, 2010) (slip op., at 6). In making this statement, the Board further emphasized the need to resolve the factual inquiries of *Graham* in determining the obviousness of a claim. *Id.*

Moreover, even if *arguendo* the processor and controller of Borkar were analogous to the processor units and controller means of claim 1, separating the dedicated processor from the remaining components of the electronic control unit taught in the alleged prior art would not be a

matter of mere design choice having no effect on the functionality of the invention. No one having ordinary skill in the art at the time of the invention would have found any motivation to implement these components on separate chips, as doing so would interaction between two different chips and require additional engineering to create a reliable interface between the two chips. The advantages proposed by Applicant's claims and specifications were not known or contemplated within the ordinary skill in the art. As such, no one having ordinary skill in the art would have found any advantage to implement a dedicated processor on a separate chip from the remaining components of an electronic control unit. For at least these reasons, the subject matter of claim 1 not taught or suggested by the alleged admitted prior art or Borkar would not have been an obvious alternative arrangement or choice of design to the skilled artisan.

According to the Supreme Court, the factual inquiries set forth in *Graham* "continue to define the inquiry that controls" obviousness rejections under 35 U.S.C. § 103. *KSR Int'l v. Teleflex Inc.*, 550 U.S. 398, 407 (2007). Under the analysis required by *Graham* to support a rejection under 35 U.S.C. § 103,

> the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined.

Graham, 383 U.S. at 17-18.

While these inquiries are factual, the ultimate determination of obviousness is a conclusion of law made in view of the totality of the resolved *Graham* factors. *KSR*, 550 U.S. at 427; *Graham*, 383 U.S. at 17.

Applying the *Graham* analysis to the present rejection of claim 1, the scope and content of the prior art, as evidenced by the admitted prior art, does not include all of the claimed subject matter, particularly "at least one of the processor units and a respective controller means are

implemented on different chips," where each of a plurality of processing units "ha[s] an I/O-interface operatively connecting to a respective one of the controller means and suppl[ies] that controller means with computing power." (Claim 1).

The differences between the cited prior art and claim 1 are significant because the claimed subject matter provides features and advantages not known or available in the cited prior art. Therefore, no one having ordinary skill in the art at the time of the invention would have been arrived at the claimed subject matter based on the teachings of the alleged prior art.

Consequently, the cited prior art will not support a rejection of claim 1 under 35 U.S.C. § 103 and *Graham*, and the Office has not met its requisite burden to establish the *prima facie* obviousness of claim 1. For at least these reasons, the rejection of claim 1 and its dependent claims should be reconsidered and withdrawn.

Claim 8

Claim 8 recites:

> A method of operating an embedded processing system comprising:
> controlling a number of electronic control units with a number of interface expander controllers, ***wherein said interface expander controllers are disposed on a separate chip from said electronic control units***; and
> ***providing computing power to said interface expander controllers with a separate number of processors***.

(Emphasis added).

The alleged admitted prior art in view of Borkar also fails to render obvious the method of claim 8, because the alleged admitted prior art does not teach or suggest all of the subject matter recited in claim 8. In particular, as demonstrated above with respect to claim 1, the alleged admitted prior art fails to teach, suggest, or otherwise render obvious the subject matter

of "said interface expander controllers [being] disposed on a separate chip from said electronic control units" or "providing computing power to said interface expander controllers with a separate number of processors." (Claim 8).

Additionally, the alleged admitted prior art in view of Borkar fails to teach or suggest the user of "interface expander controllers" which control electronic control units using computing power supplied by a "separate number of processors." (*Id.*). The alleged admitted prior art simply teaches electronic control units, where each electronic control unit includes a dedicated processor, and each electronic control unit is implemented on its own ASIC. The alleged admitted prior art makes absolutely no mention of "interface expander controllers" which control individual "electronic control units" or that the interface expander controllers receive computing power from the "separate number of processors." (*Id.*). This subject matter is completely outside the scope of the teachings and suggestions of the alleged admitted prior art in view of Borkar.

Applying the *Graham* analysis to the present rejection of claim 8, the scope and content of the prior art, as evidenced by the admitted prior art, does not include all of the claimed subject matter, particularly "said interface expander controllers [being] disposed on a separate chip from said electronic control units" or "providing computer power to said interface expander controllers with a separate number of processors." (Claim 8).

The differences between the cited prior art and claim 8 are significant because the claimed subject matter provides features and advantages not known or available in the cited prior art. Therefore, no one having ordinary skill in the art at the time of the invention would have been arrived at the claimed subject matter based on the teachings of the alleged prior art.

Consequently, the cited prior art will not support a rejection of claim 8 under 35 U.S.C. § 103 and *Graham*, and the Office has not met its requisite burden to establish the *prima facie* obviousness of claim 8. For at least these reasons, the rejection of claim 8 and its dependent claims should be reconsidered and withdrawn.

3. Claim 5 stands rejected under 35 U.S.C. § 103(a) as being allegedly obvious over the alleged admitted prior art in view of U.S. Patent No. 6,408,407 to Sadler. This rejection is respectfully traversed and should be reconsidered and withdrawn for at least the same reasons given above in favor of the patentability of independent claim 1. *See In re Fine*, 837 F.2d 1071, 1076, 5 USPQ2d 1596 (Fed. Cir. 1988) (if an independent claim is nonobvious, then any claim depending therefrom is nonobvious); M.P.E.P. § 2143.03.

Furthermore, this rejection is improper because claim 1 is rejected using the Borkar reference, and the rejection of claim 5 is not made using the Borkar reference. Thus, no *prima facie* case of obviousness has been established against claim 5 because the Examiner has failed to identify where the subject matter of claim 1 rejected based on the Borkar reference is thought to be present in the alleged admitted prior art or Sadler. Consequently, for at least these additional reasons, the rejection of claim 5 is improper and should be reconsidered and withdrawn.

4. Claim 6 stands rejected under 35 U.S.C. § 103(a) as being allegedly obvious over the alleged admitted prior art in view of U.S. Patent No. 6,222,484 to Seiple. This rejection is respectfully traversed and should be reconsidered and withdrawn for at least the same reasons given above in favor of the patentability of independent claim 1. *See Fine*, 837 F.2d at 1076 (if

an independent claim is nonobvious, then any claim depending therefrom is nonobvious); M.P.E.P. § 2143.03.

Furthermore, this rejection is improper because claim 1 is rejected using the Borkar reference, and the rejection of claim 6 is not made using the Borkar reference. Thus, no *prima facie* case of obviousness has been established against claim 6 because the Examiner has failed to identify where the subject matter of claim 1 rejected based on the Borkar reference is thought to be present in the alleged admitted prior art or Sadler. Consequently, for at least these additional reasons, the rejection of claim 6 is improper and should be reconsidered and withdrawn.

5. Claim 9 stands rejected under 35 U.S.C. § 103(a) as being allegedly obvious over the alleged admitted prior art in view of Coteus. This rejection is respectfully traversed and should be reconsidered and withdrawn for at least the same reasons given above in favor of the patentability of independent claim 8. *See Fine*, 837 F.2d at 1076 (if an independent claim is nonobvious, then any claim depending therefrom is nonobvious); M.P.E.P. § 2143.03.

Furthermore, this rejection is improper because claim 8 is rejected using the Borkar reference, and the rejection of claim 9 is not made using the Borkar reference. Thus, no *prima facie* case of obviousness has been established against claim 9 because the Examiner has failed to identify where the subject matter of claim 8 rejected based on the Borkar reference is thought to be present in the alleged admitted prior art or Sadler. Consequently, for at least these additional reasons, the rejection of claim 9 is improper and should be reconsidered and withdrawn.

Additionally, claim 9 recites "selectively providing communication between said interface expander controllers and said processors with a General Controller Unit." However, as

amply demonstrated above with respect to claim 8, the alleged admitted prior art in view of Coteus fails to teach or suggest the use of separate "interface expander controllers" to control electronic control units at all. Consequently, the admitted prior art in view of Coteus *cannot* teach or suggest "selectively providing communication between said interface expander controllers and said processors with a General Controller Unit." (Claim 9). By asserting otherwise, the Examiner is unfairly and improperly reading subject matter from the prior art that simply does not exist. Thus, for at least this additional reason, the rejection of claim 9 is improper and should be reconsidered and withdrawn.

6. Claim 10 stands rejected under 35 U.S.C. § 103(a) as being allegedly obvious over the alleged admitted prior art in view of European Patent Publication 1136325 by Denso. This rejection is moot in light of the cancellation of claim 10.

7. Claim 12 stands rejected under 35 U.S.C. § 103(a) as being allegedly obvious over Coteus in view of U.S. Patent No. 5,434,998 to Akai et al. ("Akai"). This rejection is respectfully traversed and should be reconsidered and withdrawn for at least the same reasons given above with respect to the patentability of independent claim 11. *See Fine*, 837 F.2d at 1076 (if an independent claim is nonobvious, then any claim depending therefrom is nonobvious); M.P.E.P. § 2143.03.

8. Claims 13-16 stand rejected under 35 U.S.C. § 103(a) as being allegedly obvious over Coteus in view of Akai and Sadler. This rejection is respectfully traversed and should be

reconsidered and withdrawn for at least the same reasons given above with respect to the patentability of independent claim 11. *See Fine*, 837 F.2d at 1076 (if an independent claim is nonobvious, then any claim depending therefrom is nonobvious); M.P.E.P. § 2143.03.

9. Claim 17 stands rejected under 35 U.S.C. § 103(a) as being allegedly obvious over Coteus in view of Akai, Sadler, and U.S. Patent No. 5,150,466 to Barlow et al. ("Barlow"). This rejection is respectfully traversed and should be reconsidered and withdrawn for at least the same reasons given above with respect to the patentability of independent claim 11. *See Fine*, 837 F.2d at 1076 (if an independent claim is nonobvious, then any claim depending therefrom is nonobvious); M.P.E.P. § 2143.03.

Additionally, claim 17 recites that "said ASIC stores instructions for prioritizing said application-specific controller subsystems." In this regard, the Action cites to Barlow's teaching of prioritizing "high performance I/O subsystems" at higher positional priorities on an I/O bus than low performance I/O subsystems. (Action, p. 16) (citing Barlow, col. 7 lines 16-21). However, the I/O subsystems of Barlow are clearly not the same as the "application-specific controller subsystems" recited in claim 17. The I/O subsystems of claim 17 are not application-specific, as any application may use the same I/O subsystem to transmit or receive data. Furthermore, the I/O subsystems are not controllers. Consequently, for at least these additional reasons, no *prima facie* case of obviousness has been established against claim 17, and the rejection of claim 17 should be reconsidered and withdrawn.

10. Claims 18-19 stand rejected under 35 U.S.C. § 103(a) as being allegedly obvious over Coteus in view of Akai, Salder, and Seiple. This rejection is respectfully traversed and should be reconsidered and withdrawn for at least the same reasons given above with respect to the patentability of independent claim 11. *See Fine*, 837 F.2d at 1076 (if an independent claim is nonobvious, then any claim depending therefrom is nonobvious); M.P.E.P. § 2143.03.

Additionally, claims 18-19 recite subject matter related to wirelessly transmitting a current location of an ASIC device to a recipient. In this regard, the Action cites to Seiple's teaching of a personal emergency location system in which a GPS system transmits coordinates of a person to a receiver. (Action, pp. 17-18) (citing Seiple, col. 2 lines 49-51). However, this teaching in Seiple does not render the subject matter of claims 18-19 obvious. Seiple is not analogous art to claims 18-19, as it is not reasonably pertinent to the problem with which claims 18-19 are concerned, and it is not from the same field of endeavor as claims 18-19. *See* 35 U.S.C. § 103; *In re Clay*, 966 F.2d 656 (1992) (analogous art under 35 U.S.C. § 103 must be either from the same field of endeavor or reasonably pertinent to the particular problem with which the inventor is involved). The Action's assertion that Seiple is relevant art because it teaches "the use of ASICs" is overly broad and inconsistent with the established rules of determining what is "analogous art" within the meaning of § 103. Consequently, no *prima facie* case of obviousness has been established against claims 18-19. For at least these additional reasons, the rejection of claims 18-19 should be reconsidered and withdrawn.

11. Claim 20 stands rejected under 35 U.S.C. § 103(a) as being allegedly obvious over Coteus in view of Akai, Sadler, Seiple, and U.S. Patent No. 5,475,269 to Takeuchi ("Takeuchi").

This rejection is respectfully traversed and should be reconsidered and withdrawn for at least the same reasons given above with respect to the patentability of independent claim 11. *See Fine*, 837 F.2d at 1076 (if an independent claim is nonobvious, then any claim depending therefrom is nonobvious); M.P.E.P. § 2143.03.

Additionally, claim 20 recites that "said transmitter circuitry comprises a condenser device configured to power said transmitter circuitry if a main source of power for said ASIC device is lost." In this regard, the Action cites to Takeuchi's teaching of a condenser that acts as a backup power source for the use of a microcomputer. (Action, p. 19) (citing Takeuchi, col. 1 lines 51-52). However, this portion of Takeuchi fails to teach or suggest the use of a condenser to power the transmitter in the event that power to the rest of an ASIC is lost. (*See* claim 20). Consequently, no *prima facie* case of obviousness has been established against claim 20. For at least these additional reasons, the rejection of claim 20 should be reconsidered and withdrawn.

Conclusion

In view of the preceding arguments, all claims are believed to be in condition for allowance over the prior art of record. Therefore, this response is believed to be a complete response to the Office Action. However, Applicant reserves the right to set forth further arguments in future papers supporting the patentability of any of the claims, including the separate patentability of the dependent claims not explicitly addressed herein. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed.

The absence of a reply to a specific rejection, issue or comment in the Office Action does not signify agreement with or concession of that rejection, issue or comment. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment. Further, for any instances in which the Examiner took Official Notice in the Office Action, Applicants expressly do not acquiesce to the taking of Official Notice, and respectfully request that the Examiner provide an affidavit to support the Official Notice taken in the next Office Action, as required by 37 CFR 1.104(d)(2) and MPEP § 2144.03.

If the Examiner has any comments or suggestions which could place this application in better form, the Examiner is requested to telephone the undersigned attorney at the number listed below.

Respectfully submitted,

/Steven L. Nichols/

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